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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,012	02/11/2004	Richard W. Foote	P05792	3404

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EXAMINER	
FULK, STEVEN J	
ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,012	FOOTE ET AL.	
	Examiner	Art Unit	
	STEVEN J. FULK	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-10,13-17,20,21 and 43-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10,13-17,20,21 and 43-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 22, 2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 7, 8, 10, 13-17, 20 and 43-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Matthews (US 5,108,945).

Where product-by-process limitations are recited, the claims are limited only by the structure implied by the steps, not the manipulations of the steps. For example, anticipation of claim 7 does not require that the doping be performed by implantation (in-situ doping would result in the same structure); anticipation of claim 7, 13, 16 and 45-47 does not require the doping to be performed simultaneously; anticipation of claim 17 does not require etching to separate the source and drain (masked deposition would result in the same structure).

Regarding claims 1, 4 and 43, Matthews discloses a semiconductor apparatus comprising at least one NPN double poly bipolar transistor (fig. 13B, NPN transistor 20) and at least one PMOS double poly metal oxide semiconductor transistor (fig. 13A, P-channel FET 40), wherein a base of the double poly bipolar transistor (fig. 14B, base 35) contains a first dopant having a first dopant concentration (doped using implant 42 of boron) and a gate of the double poly metal oxide semiconductor transistor contains the first dopant having the first dopant concentration (fig. 14A, doped using same implant 42 of boron); wherein an emitter (fig. 14B, 67) of the double poly bipolar transistor contains a second dopant (n-type dopant) having a second dopant concentration (col. 14, lines 28-33;n-type dopant concentration of $3.0X10^{15}$) and a source/drain (fig. 13A, 68/69) of the double poly metal oxide semiconductor transistor contains the second dopant (n-type dopant) having the second dopant concentration (col. 14, lines 51-55; n-type dopant concentration of $3.0X10^{15}$); wherein the semiconductor apparatus further comprises a first polysilicon layer (figs. 7A/B, 31) and a second silicon layer that is separate from the first polysilicon layer (figs. 11A/B, 58).

Regarding claims 2 and 44, the reference discloses the double poly bipolar transistor and the double poly metal oxide semiconductor transistor to comprise a substrate (fig. 7A, 10) and a first layer of polysilicon material (figs. 7A/B, 31), wherein: the first layer of polysilicon material in the double poly bipolar transistor is doped with impurity ions of the first dopant to form an extrinsic base (fig. 14B, 35); and the first layer of polysilicon material in the double poly MOS transistor is doped with impurity ions of the first dopant to form a MOS transistor gate (fig. 14A, 33).

Regarding claims 7, 8, 10 and 46, the reference discloses the substrate is implanted with impurity ions of a third dopant to form an intrinsic base (fig 10B, 50; col. 12, lines 41-45, boron at a concentration of $1.0X10^{14}$) in the at least one double poly bipolar transistor; and the substrate is simultaneously implanted with impurity ions to form a self-aligned lightly doped drain (fig. 10A, 53/54; col. 12, lines 30-56) in the at least one double poly MOS transistor.

Regarding claims 13-15, 17, 20 and 45, the reference discloses the at least one double poly bipolar transistor and the at least one double poly metal oxide semiconductor transistor further comprise a second layer of polysilicon material (figs. 11A/B, 58); wherein the second layer of polysilicon material in the double poly bipolar transistor is doped with impurity ions of the second dopant to form a self-aligned emitter (fig. 13B, 67; doped with n-type dopant at $3.0X10^{15}$); and the second layer of polysilicon material in the double poly MOS transistor is doped with impurity ions of the second dopant to form a self-aligned MOS source/drain (fig. 13A, 68/69; col. 14, lines 51-55; n-type dopant concentration of $3.0X10^{15}$).

Regarding claims 16 and 47, the reference discloses the second layer of polysilicon material in the at least one double poly bipolar transistor is doped with impurity ions to form a deep collector (fig. 15B, 84).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews (US 5,108,945) in view of Maeda et al. (US 5,091,760).

Matthews discloses all of the elements of the claim(s) as set forth in paragraph 3 above, and Matthews also teaches forming an NMOS transistor (fig. 13A, 30), but the reference does not explicitly disclose forming a PNP bipolar transistor device. Maeda discloses a semiconductor apparatus comprising a substrate (fig. 1G, 10), at least one PNP double poly bipolar transistor that comprises a first polysilicon layer doped with impurity ions to form an extrinsic base (figs. 1G & 1H, PNP device with base in first poly layer 58 and emitter in second poly layer 37) and at least one NMOS double poly metal oxide semiconductor transistor with a first layer of polysilicon material doped with impurity ions to form an MOS transistor gate (figs. 1G &1H, NMOS device with gate in first poly layer 50 and source/drain in second poly layer 39); further comprising a second polysilicon layer, wherein the second layer of polysilicon material in the at least one double poly bipolar transistor is doped with impurity ions to form an emitter (fig. 1H, 37); and the second layer of polysilicon material in the at least one double poly MOS transistor is doped with impurity ions to form a MOS source/drain (fig. 1H, 39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the PNP bipolar transistor of Maeda in the method of forming a BiCMOS device of Matthews. One would have been motivated to do this because Maeda taught that forming a PNP bipolar device in addition to the NPN, PMOS and NMOS devices of a BiCMOS circuit would allow the device capacitance to be reduced, thus increasing the operating speed of the circuit (Maeda, fig. 2C; col. 6, lines 19-32).

Response to Arguments

6. Applicant's arguments with respect to the rejection of claims 1, 2, 4, 7, 8, 10, 13-17 and 20 over Matthews '945 have been fully considered but they are not persuasive. Applicant argues that the emitter (67) of the bipolar device of Matthews is formed after the source (68) and drain (69) of the MOS device. This argument is irrelevant because claim 1 is directed toward a product, and thus the claim is limited only by the structure, and not by the order or manipulation of the steps to form the product. Applicant further argues that Matthews teaches the emitter to be formed by a dopant (Arsenic) that is different from the dopant (Boron) of the source/drain. However, claim 1 only requires that the same "dopant" is used with the same concentration. The dopants in the emitter (67) and the source/drain (68/69) are both n-type, and are therefore considered the same. The exact element used for the n-type dopant is not claimed. Further, the concentration of both n-type dopants are also disclosed to be the same.

7. Applicant's arguments with respect to claims 3, 9 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN J. FULK whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Rose can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven J. Fulk/
Examiner, Art Unit 2891